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CR23X CALIBRATION & CHECK-OUT PROCEDURES

1.0 Purpose

1.1 To describe the procedure for performing CR23X calibration.
1.2 To verify product functionality.

2.0 Scope

2.1 Applies only to the CR23X Datalogger.

3.0 Test Equipment Needed

3.1 Adjustable 12V Power Supply
3.2 Function Generator
3.3 Voltmeter (5 ½ Digit)
3.4 Frequency Counter
3.5 Oscilloscope
3.6 DC Voltage Calibrator
3.7 Current Monitor

4.0 Calibration Procedures

1-Current drain:
Check quiescent current. The CR23X quiescent current should be less than 2.1 mA at room temperature with the display off(*0 #). Low resistance resistors are provided on each supply to determine the current that the supply is sourcing or sinking.

2-Set Clock Compensation:
The 9.830MHz CPU clock needs to be compensated for in software. This is accomplished by doing the following. Measure the frequency at test point C16Q1. This point is just below the CPU clock crystal. Make note of the frequnecy, (resolution to 1Hz). The ideal frequency at the test point is 2.457600MHz. Subtract the measured value from the ideal. If the measured value is less than the ideal, subtract the difference of the two numbers from 1600. If the measured value is greater than the ideal, add the difference to 1600. Using the CS I/O port take the datalogger into telcom; type in the following sequence of numbers (19287P enter will show what difference has been loaded in) (19287:1550P enter will load the new number in). The 1550 represents a difference of 50 Hz from the ideal of 1600. If done properly two numbers will appear on the screen. The first number will be very close to the actual number in Hz that is being compensated for. Always check clock compensation after loading a new Operating System.

3-Set The 32.768 kHz clock:
Connect a frequency counter to test point C15M. Adjust pot C17M to the frequncy of 32.768 kHz with a resolution better than plus or minus .01Hz (example of acceptable values include 32768.005 Hz, or a period lower than 30.517569us and higher than 30.5175873us).

4-Instrumentation Amplifier (IA) Offset Voltage:
First trim the IA offset voltage by means of trim pot R24G and P24. Use *A Index parameter 1(input storage loctions) set to at least 32 input locations. Then do P24 with option code 2, trim pot so that P24 offset value for ± 10 mV input range (Loc. 8) (IA gain = 100) is within ± 20 counts of zero.

5-DAC ZERO

Next trim out the DAC and excitation voltage offsets by utilizing an Excitation with Delay (P22) instruction as follows:

	Ex. Chan	Del w/ex 0.01s	Del after/ex 0.01s	EXIT mV
P22	1	9999	0	0

A: Hook the voltmeter ground to any ground terminal that is associated with single ended or differential channels; do not use the grounds that are next to the Exitation out and CAO outs. Connect the positive lead to test point (C23L) for VDAC offset trim. Adjust pot (R24I) to 0.000 mV ± 0.05 mV on the voltmeter on a ± 200 mV or smaller input voltage range.
B: Next trim excitation offset by hooking voltmeter positive lead to the EX1 output terminal on the panel and adjust pot (R14K) to 0.000 mV ± 0.05 mV on the voltmeter on a ± 200 mV or smaller input voltage range.

6-DAC Reference:

The ± 5.46 V voltage measurement reference is trimmed with pots (R21I) at +4000 mV followed by trimming pot (R21L) for -4000 mV. This trim is accomplished with an accurate **DC voltmeter.** With the voltmeter hooked to the EX1 terminal and the datalogger's iput channel ground (not ground terminal next to it), trim ± 5.46 V reference by setting P22 DAC output to +4000 mV and trimming pot (R21I) so that the EX1 output reads within +4000.0 mV ± 0.5 mV (3999.5 mV to 4000.5 mV). Then change excitation in P22 to -4000.0 mV and trim pot (R21L) for the EX1 output to read within -4000.0 mV ± 0.5 mV (-3999.5 mV to 4000.5 mV).